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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,995	01/09/2006	Andrea Milanesi	DE03 0240 US1	7025
65913	7590	04/29/2010		
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER MORRIS, JOHN J	
			ART UNIT 2629	PAPER NUMBER
			NOTIFICATION DATE 04/29/2010	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/563,995	MILANESI, ANDREA	
	Examiner	Art Unit	
	John Morris	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 7-13 and 15 is/are rejected.
- 7) ☐ Claim(s) 4, 6 and 14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 4, 6, and 14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 5-10, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brokaw (US Pat# 6040732) in view of Huijsing et al. (US Pat# 4555673/ *or* "Huijsing" hereinafter).

For **claim 1**, Brokaw teaches an input stage with a transistor doublet having a first differential input for receiving input signals (Q20, Q14), a second transistor doublet

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having a second differential input for receiving input signals (Q1, Q5), and a plurality of switches for receiving and selectively directing analog input signals only to one of either said first differential input or to said second differential input responsive to a switching signal and for connecting the other one of the first and second differential inputs to a reference voltage responsive to the switching signal (Brokaw, figure 5).

Brokaw does not teach the transistors doubles to be a PMOS and a NMOS doublet and whereby the input stage is configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant.

However, in the same field of endeavor, Huijsing teaches an apparatus comprising an input stage with an NMOS transistor doublet having a first differential input for receiving input signals and a PMOS transistor doublet having a second differential input for receiving input signals (Huijsing, figure 2). Huijsing also teaches constant transconductance (Huijsing, abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Brokaw with Huijsing because both deal with amplifiers and the addition of the switches would reduce power consumption.

For **claim 3**, Brokaw teaches wherein one transistor doublet (Q20, Q14) comprises two transistors, each having a gate, whereby the gate of the first of the two transistors is connectable to a first input (ENABLE0) node via a first switch of the plurality of switches and the gate of the second of the two transistors is connectable to a

second input (VIN)) node via a second switch of the plurality of switches, the second transistor doublet (Q1, Q5) comprises two transistors, each having a gate, whereby the gate of the first of the two transistors is connectable to the first input (ENABLE0) node via a third switch of the plurality of switches and the gate of the second of the two transistors is connectable to the second input (VIN1) node via a fourth switch of the plurality of switches (Brokaw, figure 5). Brokaw does not have a switch directly connected to the input of the transistor doubles and their second input node directly connected to VIN0 and VIN1; however, these inputs are *connectable* to switches if one decides to place a switch there.

For **claim 5**, Huijsing teaches a rail-to-rail input stage (Huijsing, abstract).

For **claim 7**, Brokaw and Huijsing do not teach a digital switch; however, the examiner takes official notice that it would have been an obvious matter of design choice to use a digital signal to control the switching circuit since the signal only needs to have two states, on and off.

For **claim 8**, Brokaw teaches that the switches can be transistors (Brokaw, figure 5).

For **claim 9**, Huijsing teaches transistor doublets as part of a folded cascade rail-to-rail input stage and wherein the folded cascade rail-to-rail input stage is connected to a second stage comprising a rail-to-rail output stage amplifier (Huijsing, figure 1 and 3b).

For **claim 10**, Brokaw and Huijsing do not teach a source driver bank; however, the examiner takes official notice that this would have obvious to one of ordinary skill in the art to have a plurality of apparatus' in a driver bank since such a modification would only require a mere replication of the apparatus. It is also well known that a bus is used for receiving input signals since a bus may only be an electrical connection use to transfer data.

For **claim 12**, Brokaw and Huijsing do not teach a control signal generator; however, it would have been obvious that there is one since control signals need to be generated for the switches to work correctly.

For **claim 15**, Huijsing teaches the first differential input is formed by the gates of the NMOS transistor doublet and the second differential input is formed by the gates of the PMOS transistor doublet (Huijsing, figure 2).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brokaw (US Pat# 6040732) in view of Huijsing et al. (US Pat# 4555673/ or "*Huijsing*" *hereinafter*) and Nishimura (US Pub# 20010004255 A1).

For **claim 2**, Brokaw and Huijsing do not teach wherein the plurality of switches direct the analog input signals to said first differential input if the input signals have positive gamma data and to said second differential input if the input signals have negative gamma data.

However, in the same field of endeavor, Nishimura teaches directing the analog input signals to said first differential input if the input signals have positive gamma data and to said second differential input if the input signals have negative gamma data (Nishimura, abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify because, as motivated by Nishimura, it would reduce power consumption (Nishimura, paragraph 37).

3. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable Brokaw (US Pat# 6040732) in view of Huijsing et al. (US Pat# 4555673/ or "*Huijsing*" *hereinafter*) and Miyazawa et al. (US Pub# 20020196247 A1/ or "*Miyazawa*" *hereinafter*).

For **claim 13**, Miyazawa teaches that the circuit is part of a display panel module (Miyazawa, page 5, paragraph [0063], lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Brokaw and Huijsing with Miyazawa because the addition would allow for an increase in control as to which transistor pairs to use.

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4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brokaw (US Pat# 6040732) in view of Huijsing et al. (US Pat# 4555673/ or "*Huijsing*" *hereinafter*) and applicant admitted prior art (*AAPA hereinafter*).

For **claim 11**, Brokaw and Huijsing do not teach a gate driver bank or an LCD panel; however, in the same field of endeavor, AAPA teaches that it is prior art for a conventional LCD to comprise of a gate driver bank and an LCD panel (AAPA, figure 4). AAPA also teaches a standard rail-to-rail input stage circuit (which Huijsing teaches) used in LCD (AAPA, figure 3). Therefore, it would have been obvious to modify Huijsing to be included in a conventional LCD driver circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Brokaw and Huijsing with AAPA because all deal with the same subject matter and the addition of the AAPA would increase the effectiveness of the gate driver.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morris whose telephone number is (571)270-7171. The examiner can normally be reached on Monday-Friday, 7am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amr Awad/

Supervisory Patent Examiner, Art Unit 2629